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(54) Integrated circuit multilevel metallization and method for making same

(57) The first metal interconnect layer of a multilayer integrated circuit is produced by depositing a first metallization layer of aluminum copper (12) followed by depositing a second metallization layer of pure aluminum (16) on top of the aluminum copper (12). This reduces the stress related defects such as micropits and microvoids. Alternatively the first metallization layer may comprise aluminium silicon, aluminium copper silicon, titungsten or a silicide thereof, and the second metallization layer may comprise any conductive metal, but should be of different composition from that of the first metallization layer.

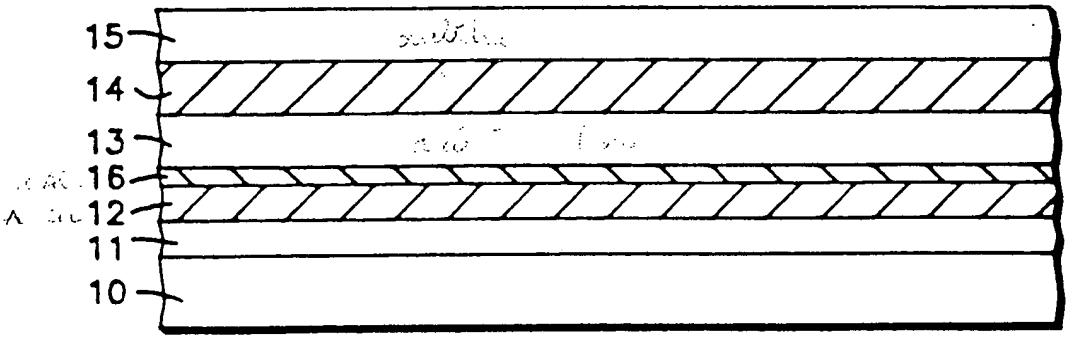

FIG. 2

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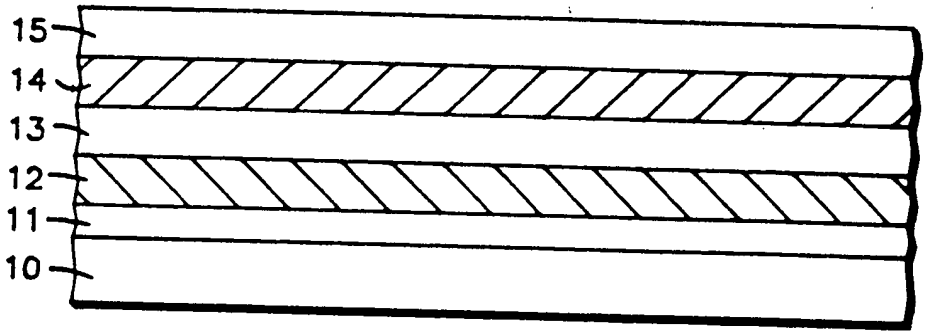

FIG. 1 - PRIOR ART -

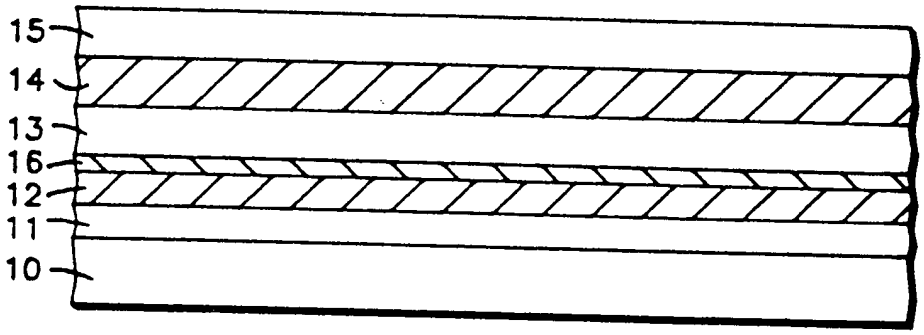

FIG. 2

SPECIFICATION

Integrated circuit multilevel metallization and method for making same

Background of the Invention

This invention relates, in general, to improving the yields in the manufacturing of semiconductor multilayer integrated circuits, and more particularly, to the prevention of stress induced defects found in such circuits.

Integrated circuits are built on substrates usually made of silicon. The silicon substrate is subdivided into chips or die. It is within the die that thousands of devices (e.g. diodes, transistors, resistors) are manufactured. To help decrease the cost of an integrated circuit, the density of the die is increased by shrinking the device size, and the line widths, and increasing the number of devices in a given die size. To aid in the condensing of devices, the metal interconnects have gone from a single layer design to a dual or multilevel design which are commonly called multilayer metalization.

One of the formidable problems in multilayer metallization is the stress that is created by placing a layer of metal between two layers of dielectrics. Two known defects that are usually associated with this type of stress are micropits and microvoids.

As used herein, "micropit" refers to a microscopic depression in the conductive layer that does not penetrate entirely through it. The term "microvoid" is used to mean the absence of metal micrscopic in size in a localized region.

The use of aluminum alloys, for example, aluminium copper or aluminum copper silicon, has many advantages with respect to electomigration, hillock growth and fine line geometries. However, aluminum and aluminum alloys have a relatively large thermal mismatch with the dielectrics that isolate the aluminum alloy from above and below. It is this thermal mismatch that creates a stress between the aluminum and the dielectrics which sometimes leads to the cracking of the dielectric and frequently creates micropits and microvoids in the first level aluminum metal interconnect.

Summary of the Invention

Accordingly, it is an object of this invention is to decrease or eliminate micropits and microvoids through the use of a dual metal film for the first metal level interconnect in a multilayer circuit.

A further object of this invention is to provide improved integrated circuits by having fewer rejects from stress related defects.

The foregoing and other objects and advantages are achieved in the present invention which, as part thereof, makes use of a method for forming a multilevel metallization on a semiconductor substrate which comprises forming a first dielectric layer over the substrate, depositing a first metallization layer over the first dielectric, depositing a second metallization layer over the first mallization layer, forming a second dielectric layer over the second metallization layer, and depositing a third metallization layer over the second dielectric layer.

Another embodiment of the present invention comprises a multilayer metallization semiconductor device in which the first layer metallization comprises; a film of conductive metal of a first composition, and a film of conductive metal of a second composition deposited over the metal of the first composition.

The features and advantages of the invention will be apparent from the following, more detailed description of the preferred embodiment of the invention taken in conjunction with accompanying drawings.

Brief Description of the Drawings

Figure 1 is an enlarged sectional view of the prior art illustrating a portion of an integrated circuit fabricated in accordance with conventional techniques and

Figure 2 is an enlarged sectional view illustrating a portion of an integrated circuit fabricated in accordance with the present invention.

Detailed Description of the Drawings

The sectional views illustrated in Fig. 1 and Fig. 2 presents a portion of an integrated circuit. For purposes of simplicity, the drawings show a substrate 10 which is understood to comprise an integrated circuit which contains active and passive components that are not shown. When reviewing the two figures, it should be noted that corresponding numbers represent the same fabrication steps and thicknesses. In addition, it should be noted that the thickness shown herein are selected for clarity of illustrating and are not to be interpreted in a limiting sense. Also, for purposes of simplicity, the photolithography and etch steps have not been included since these are well known by those of skill in the art.

Fig. 1 represents a portion of an integrated circuit which may be formed by any of the conventional methods used in the prior art. Dielectric layer 11, such as silicon nitride, is formed on top of substrate 10 to a thickness of approximately 700 nanometers (nm), and is used to isolate the components in substrate 10 from metal layer 12. Metal layer 12 such as aluminum copper, or the like, is sputter deposited on top of silicon nitride layer 11 to a thickness of approximately 700 nm. Aluminum copper layer 12 has a copper content ranging from 1.5 to 2.5 weight percent. Dielectric 13 such as plasma enhanced silicon dioxide, is deposited by a commercial plasma reactor on top of metal layer 12 to approxi-

mately 700 nm. Dielectric layer 13 is used to isolate metal layer 12 from metal silicon layer 14. Metal layer 12 is commonly referred to as the first metal interconnect and metal layer 14 is commonly referred to as the second metal interconnect. In order to provide contact between metal layer 12 and metal layer 14 contact holes are formed in select areas of dielectric layer 13. The contact holes are not shown in Fig. 1. Metal layer 14, such as aluminum copper silicon, is sputter deposited on top of silicon dioxide 13 and has a copper content ranging from 1.5 to 2.5 weight percent and a silicon content ranging from 1.0 to 2.0 weight percent. Dielectric layer 15, such as phosphosilicate glass, or the like, is deposited over metal layer 14 using chemical vapor deposition techniques that are well known in wafer processing to a thickness of 1500 nm. To provide contact to second metal layer 14 contact vias are formed in dielectric layer 15. The contact vias are not shown in Fig. 1.

The sectional view illustrated in Fig. 2 represents a portion of an integrated circuit which is formed in accordance with the teachings of the present invention.

Substrate 10, dielectric 11 and metal layer 12 are the same in Fig. 2, as in Fig. 1. Metal layer 16 such as pure aluminum, or the like, is sputter deposited on top of metal layer 12 to a thickness of approximately 100 nm thereby forming a cap over layer 12. Metal layer 16 uses an aluminum source that has a purity of 99.999 percent. It has been found that using a composite layer of two different aluminum or aluminum alloy layers such as aluminum copper 12 and aluminum 16, for the first metal layer interconnect, that the stress induced defects such as micropits and microvoids are greatly reduced or eliminated. It is believed that other aluminum alloys could be used for the composite first metal layer. One such example would be to have a layer of aluminum copper that is approximately 700 nm thick covered by approximately a 100 nm thick layer of aluminum copper silicon. Dielectric 13, metal layer 14 and dielectric 15 are the same in Fig. 2 as in Fig. 1.

Thus it is apparent that there has been provided, in accordance with the invention, an improved multilayer integrated circuit with less stress related defects due to the use of two metal films for the first metal layer instead of the one film found in the prior art. It is not clearly understood why the use of a composite first metal layer helps in reducing microvoids and micropits. It is suggested that the addition of the extra layer of metal helps bring the total stress of the wafer closer to zero. Each layer of film that is deposited on the substrate has a certain degree of thermal stress and intrinsic stress. The thermal stress is due to the difference in the thermal expansion coefficients of the coating and substrate materials. The intrinsic stress is due to the accumulating effect of the crystallographic flows that are built into the coating during deposition.

The internal stresses in a thin film can give rise to seemingly unrelated behavior that can seriously influence the films performace. Some of these behaviors include micropiting and microvoids.

Having thus described the invention, it will be apparent to those skilled in the art that various modifications can be made within the spirit and scope of the present invention. As an example, Dielectric layer 11 can comprise silicon oxide or oxynitride. First metal layer 12 can comprise aluminum silicon, aluminum copper silicon, titungsten or a silicide thereof. Metal layer 16 can be any conductive metal but should be of a different composition than that found in metal layer 12. Dielectric layer 13 can comprise quartz, phosphosilicate glass, plasma enhanced silicon nitride, polyimide or composites thereof. Second metal layer 14 could be aluminum silicon. Dielectric layer 15 can comprise plasma enhanced silicon dioxide or polyimide.

CLAIMS

1. A method for forming a multilevel metallization on a semiconductor substrate comprising:

forming a first dielectric layer over the substrate;

depositing a first metallization layer over the first dielectric layer;

depositing a second metallization layer over the first metallization layer;

forming a second dielectric layer over the second metallization layer; and

depositing a third metallization layer over the second dielectric layer.

2. The method in claim 1 wherein the first dielectric is silicon nitride.

3. The method in claim 1 wherein the first metallization is aluminum copper.

4. The method in claim 1 wherein the second metallization layer is aluminum.

5. The method in claim 1 wherein the second dielectric layer is plasma enhanced silicon dioxide.

6. The method in claim 1 wherein the third metallization layer is aluminum copper silicon.

7. A method for improving manufacturing yields of a multilayer integrated circit comprising the steps of:

forming a metallization layer over an insulating layer; and

forming a metallized cap over said metallization layer.

8. A multilayer metallization semiconductor device in which the first layer metallization comprises:

a film of conductive metal of a first composition; and

a film of conductive metal of a second composition deposited over the metal of the first

composition.

9. The device in claim 8 in which the metal of the first composition is an aluminum alloy.

10. The device in claim 8 in which the metal of the second composition is substantially pure aluminum.

CLAIMS

Amendments to the claims have filed, and have the following effect:–

Claims 1–10 above have been deleted or textually amended.

New or textually amended claims have been filed as follows:–

1. A method for improving manufacturing yields of an integrating circuit having multilayer metallization, comprising forming a first layer of metal over a first dielectric layer wherein the first layer of metal is an aluminum alloy; forming a second metal layer of substantially pure aluminum over the first layer of metal; and forming at least a second dielectric layer over the second metal layer.

2. The method of claim 1 wherein the first layer of metal is aluminum copper.

3. The method of claim 1 wherein the second metal layer has a purity of at least 99 percent.

4. A method of preventing formation of stress induced micropits in a multi layer metallization having a metal layer sandwiched between two dielectric layers comprising, forming the metal layer of a first layer of an aluminum alloy covered by a second layer of of substantially pure aluminum.

5. The method of claim 4 wherein the aluminum alloy comprises aluminum copper.

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